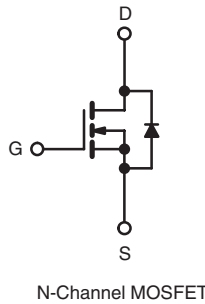
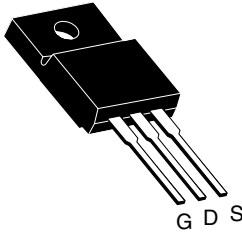


Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.320
Q_g (Max.) (nC)	92	
Q_{gs} (nC)	24	
Q_{gd} (nC)	44	
Configuration	Single	

TO-220 FULLPAK



FEATURES

- Super Fast Body Diode Eliminates the Need for External Diodes in ZVS Applications
- Lower Gate Charge Results in Simpler Drive Requirements
- Enhanced dV/dt Capabilities Offer Improved Ruggedness
- Higher Gate Voltage Threshold Offers Improved Noise Immunity
- Lead (Pb)-free



APPLICATIONS

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control Applications


ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	IRFIB7N50LPbF
	SiHFIB7N50L-E3

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	27	
Linear Derating Factor		0.37	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	550	mJ
Avalanche Current ^a	I_{AR}	6.8	A
Repetitive Avalanche Energy ^a	E_{AR}	4.6	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	46
Peak Diode Recovery dV/dt^c		dV/dt	24
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s		
Mounting Torque	6-32 or M3 screw		10
			1.1

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 12).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 24\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 6.8\text{ A}$ (see fig. 14).
- $I_{SD} \leq 6.8\text{ A}$, $dI/dt \leq 650\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $dV/dt = 24\text{ V/ns}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	2.69	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.44	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$		-	-	50	μA
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	2.0	mA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 4.1\text{ A}^b$	-	0.32	0.38	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 4.1\text{ A}$		4.7	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5		-	2220	-	pF
Output Capacitance	C_{oss}			-	230	-	
Reverse Transfer Capacitance	C_{riss}			-	23	-	
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	2780	-	pF
			$V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$	-	63	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 0\text{ V to } 400\text{ V}^c$	-	140	-	
Effective Output Capacitance (Energy Related)	$C_{oss\text{ eff. (ER)}}$			-	100	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 6.8\text{ A}, V_{DS} = 400\text{ V}$, see fig. 7 and 16 ^b	-	-	92	nC
Gate-Source Charge	Q_{gs}			-	-	24	
Gate-Drain Charge	Q_{gd}			-	-	44	
Internal Gate Resistance	R_G	$f = 1\text{ MHz}$, open drain		-	0.88	-	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}$	$V_{DD} = 250\text{ V}, I_D = 6.8\text{ A}, R_G = 9.0\text{ }\Omega$, see fig. 11a and 11b ^b	-	23	-	ns
Rise Time	t_r			-	36	-	
Turn-Off Delay Time	$t_{d(off)}$			-	47	-	
Fall Time	t_f			-	19	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	6.8	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	27	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 6.8\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 6.8\text{ A}, T_J = 125\text{ }^\circ\text{C}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	85	130	ns
				-	130	200	
Body Diode Reverse Recovery Charge	Q_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_S = 6.8\text{ A}, T_J = 125\text{ }^\circ\text{C}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	280	420	nC
				-	570	860	

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain-Source Body Diode Characteristics						
Body Diode Reverse Recovery Current	I_{RRM}	$T_J = 25^\circ\text{C}$	-	5.9	8.9	A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 12).
- b. Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2\%$.
- c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DS} .
 C_{oss} eff. (ER) is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DS} .

TYPICAL CHARACTERISTICS 25°C , unless otherwise noted

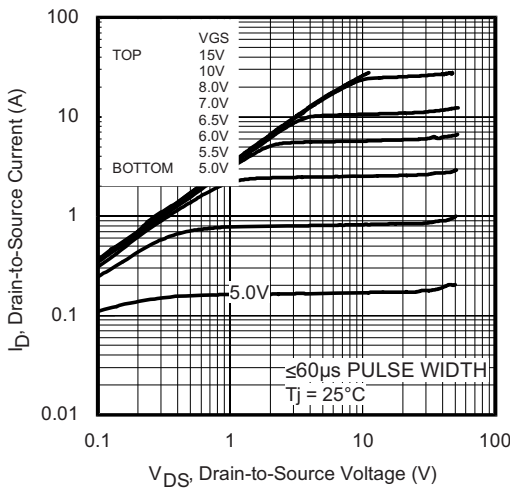


Fig. 1 - Typical Output Characteristics

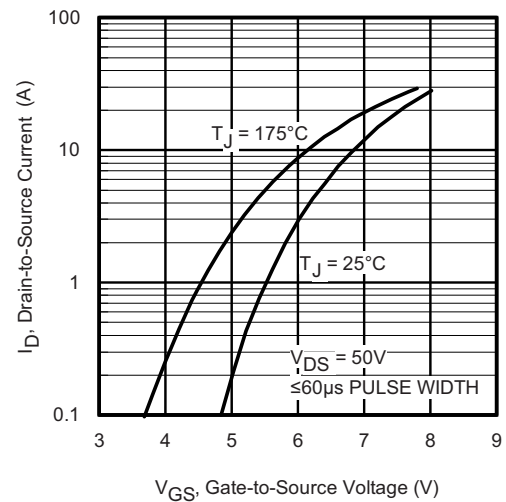


Fig. 3 - Typical Transfer Characteristics

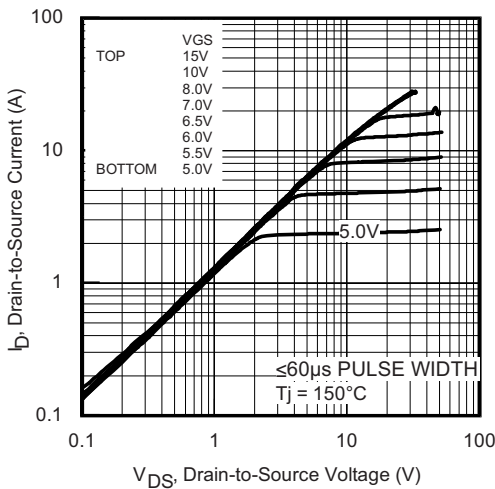


Fig. 2 - Typical Output Characteristics

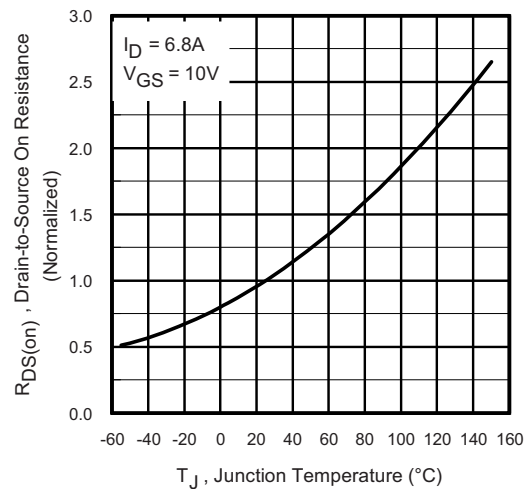


Fig. 4 - Normalized On-Resistance vs. Temperature

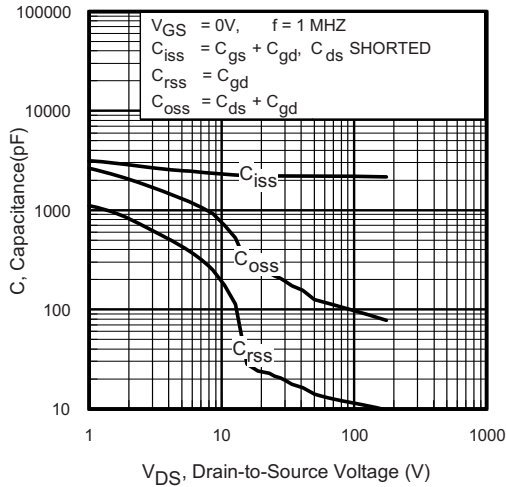


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

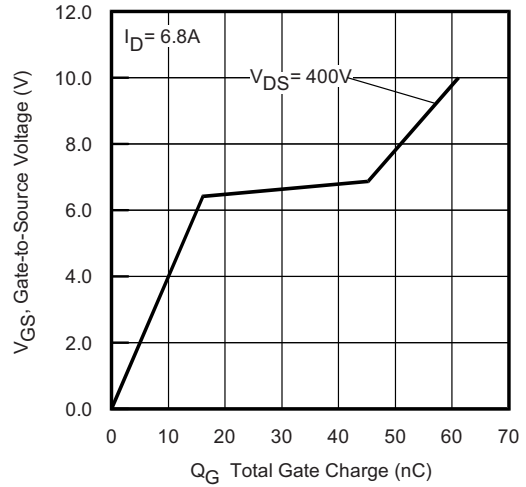


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

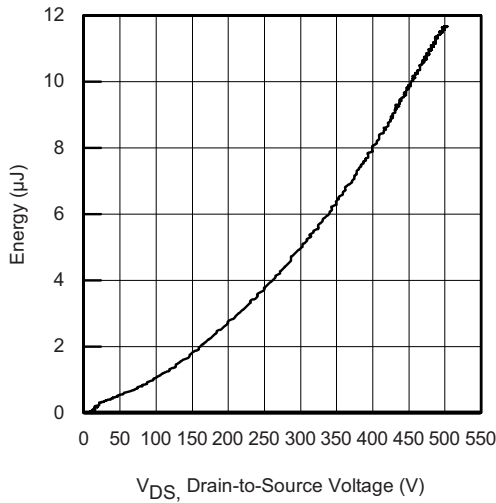


Fig. 6 - Typical Output Capacitance Stored Energy vs. V_{DS}

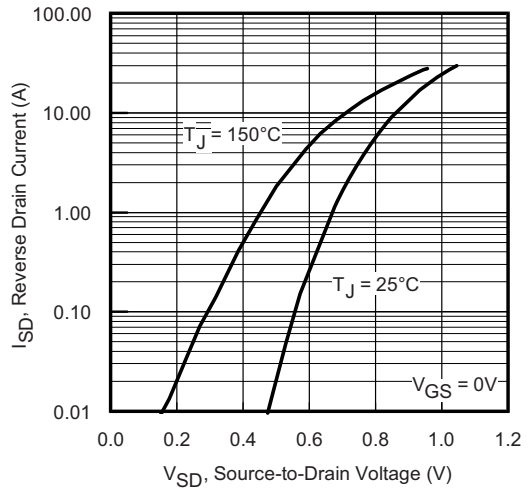


Fig. 8 - Typical Source-Drain Diode Forward Voltage

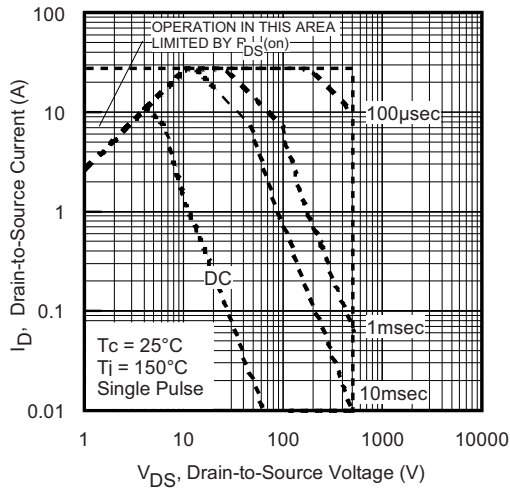


Fig. 9 - Maximum Safe Operating Area

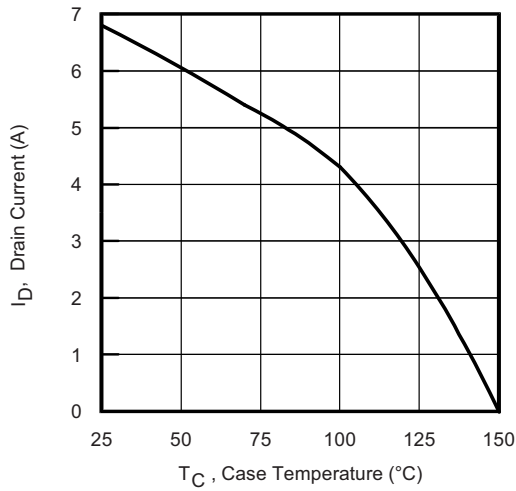


Fig. 10 - Maximum Drain Current vs. Case Temperature

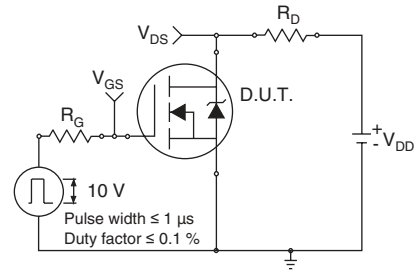


Fig. 11a - Switching Time Test Circuit

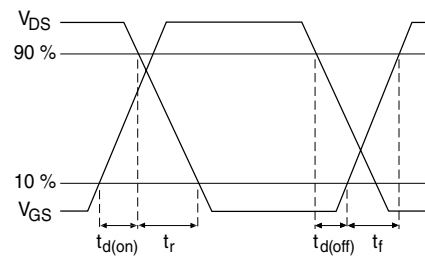


Fig. 11b - Switching Time Waveforms

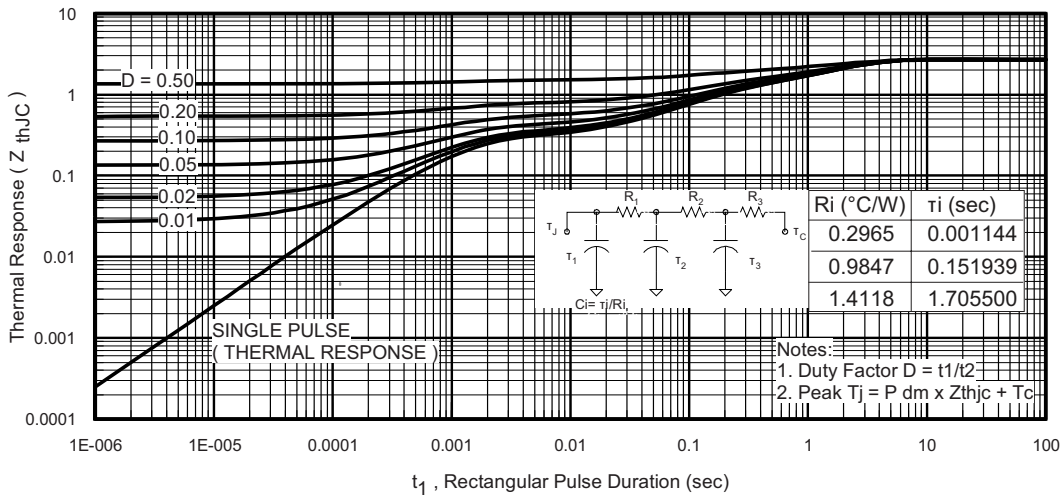


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

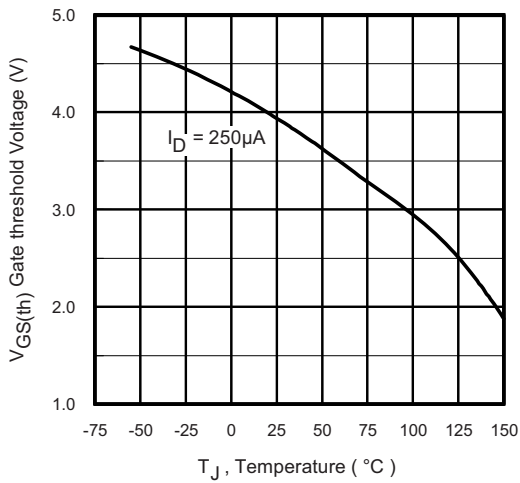


Fig. 13 - Threshold Voltage vs. Temperature

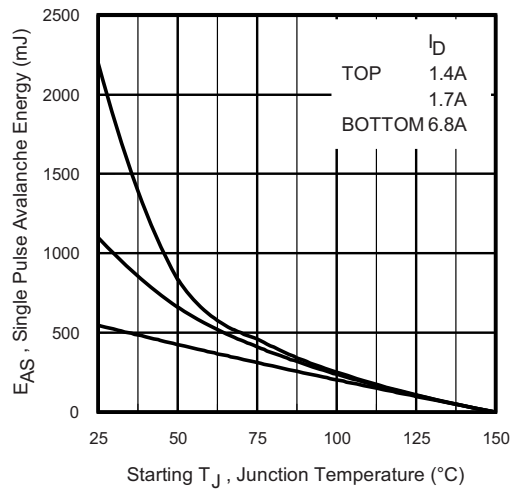


Fig. 14 - Maximum Avalanche Energy vs. Drain Current

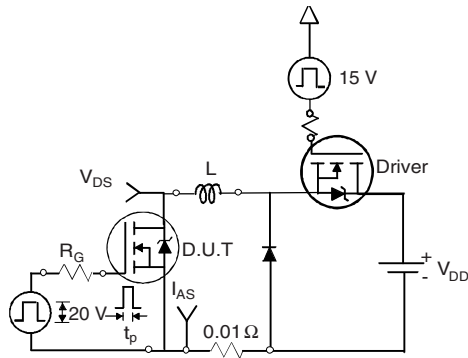


Fig. 15a - Unclamped Inductive Test Circuit

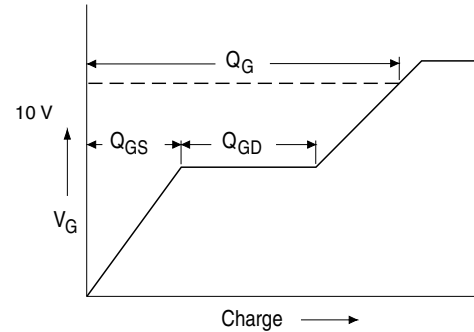


Fig. 16a - Basic Gate Charge Waveform

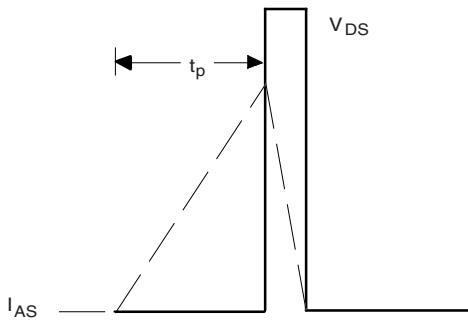


Fig. 15b - Unclamped Inductive Waveforms

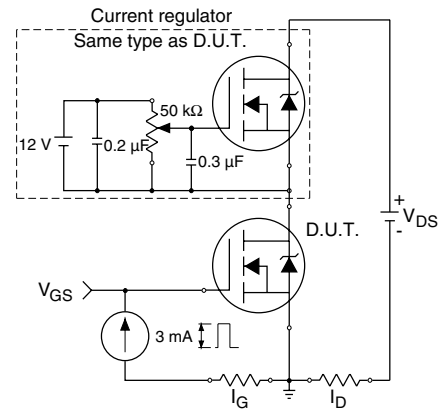
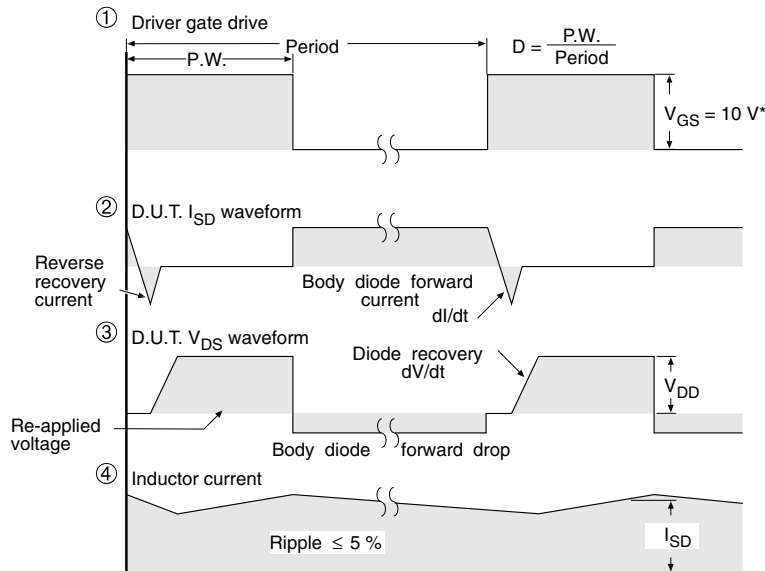
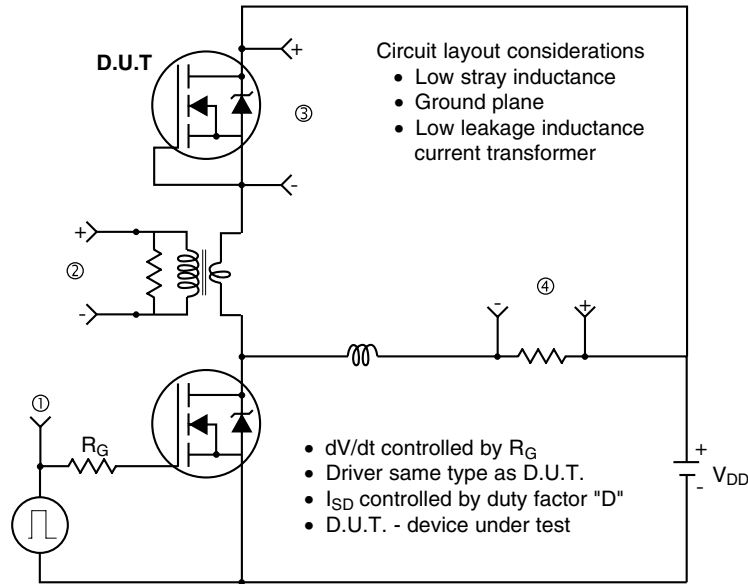


Fig. 16b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices

Fig. 17 - For N-Channel

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